

FIG. 1

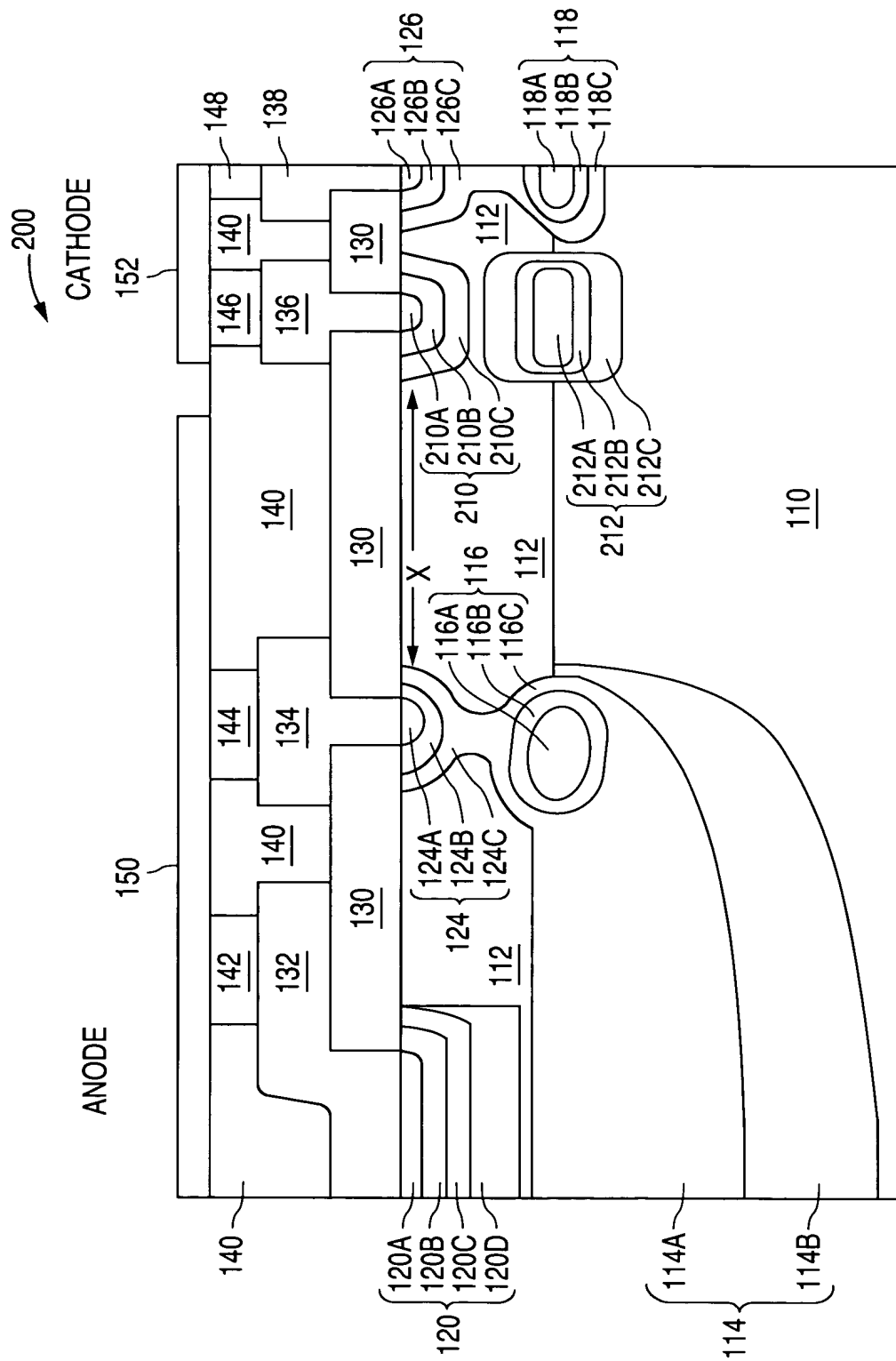


FIG. 2

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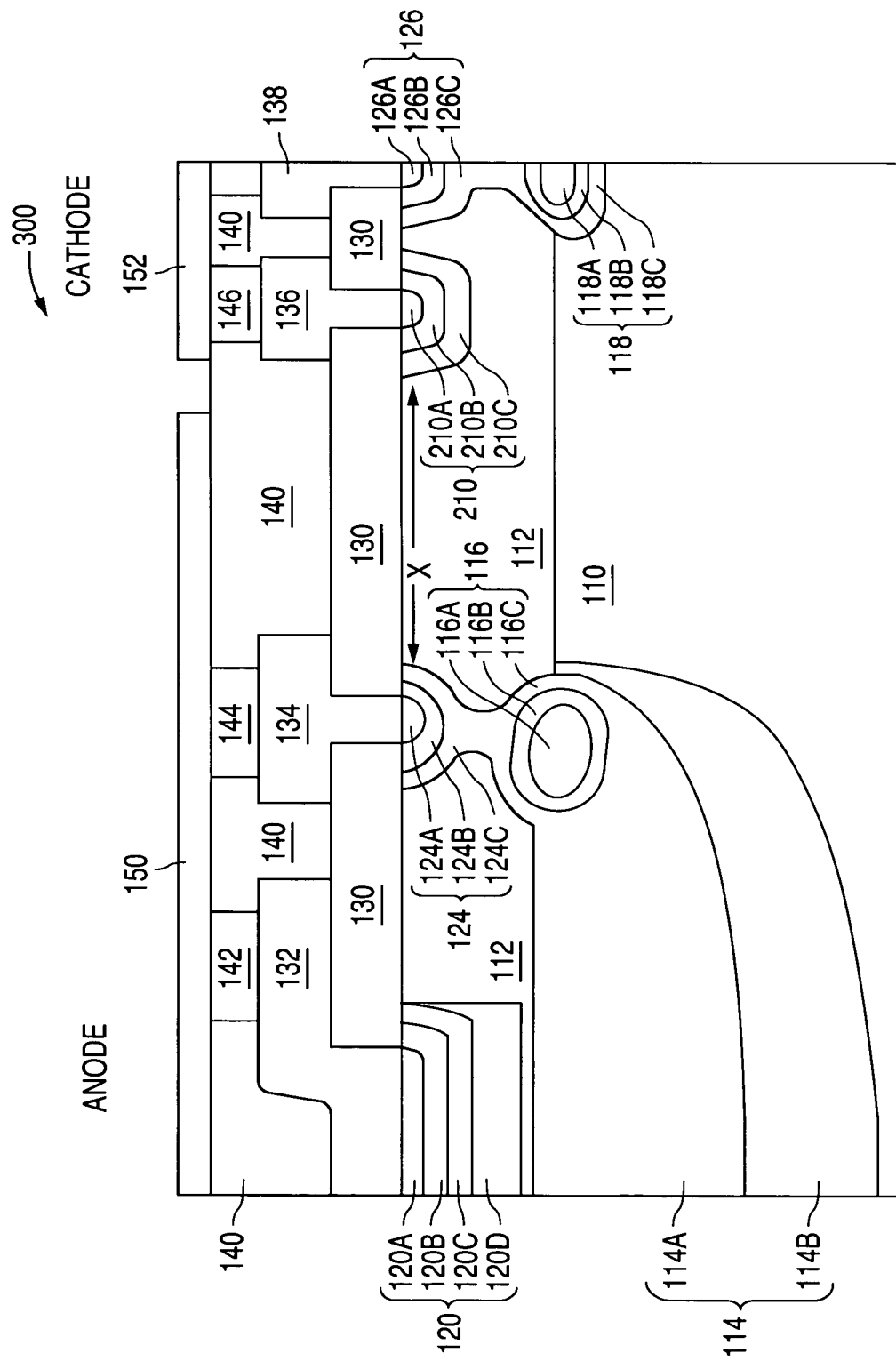


FIG. 3

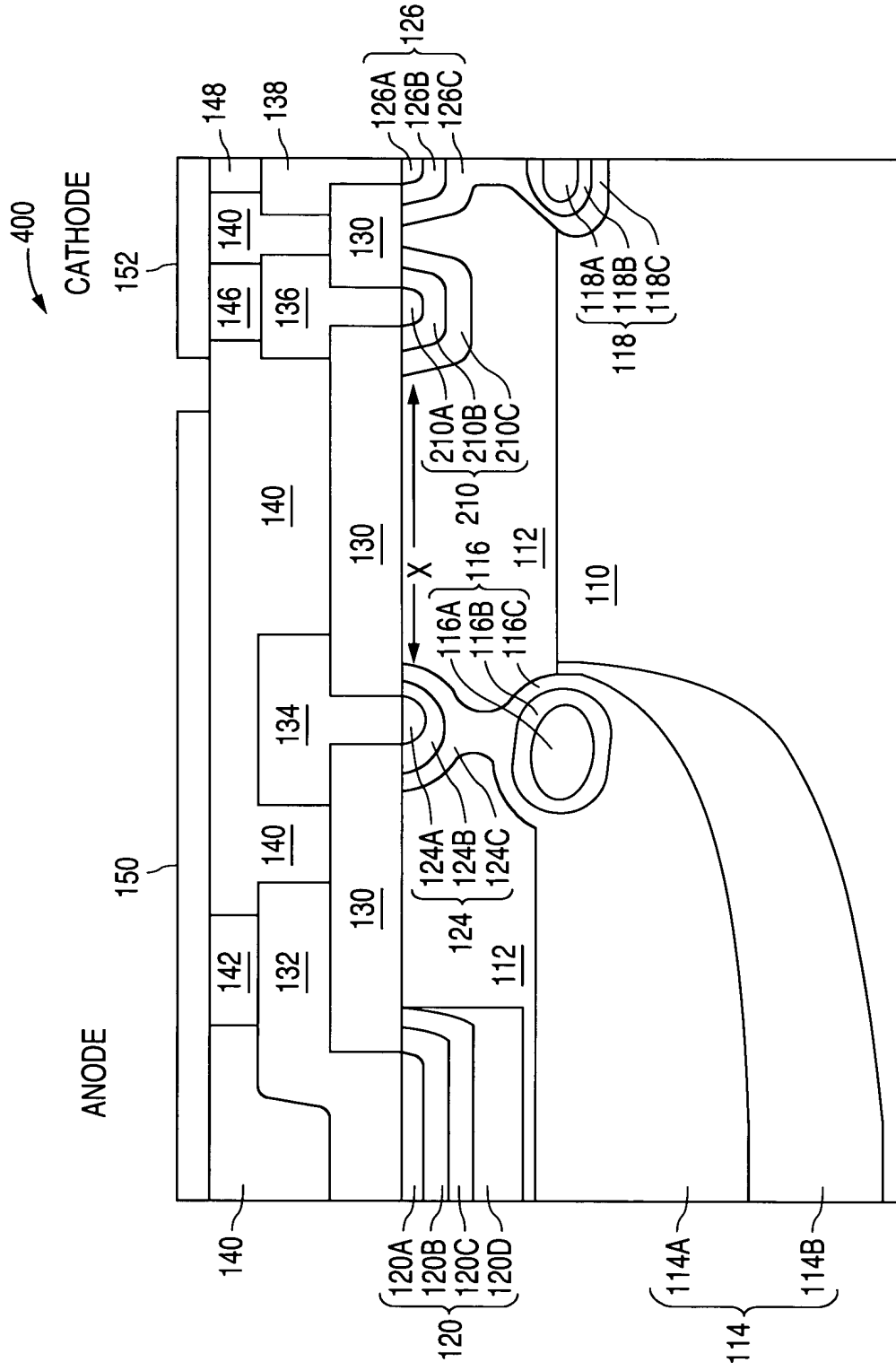
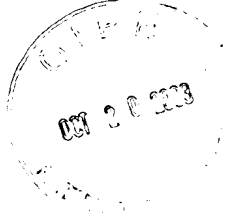


FIG. 4

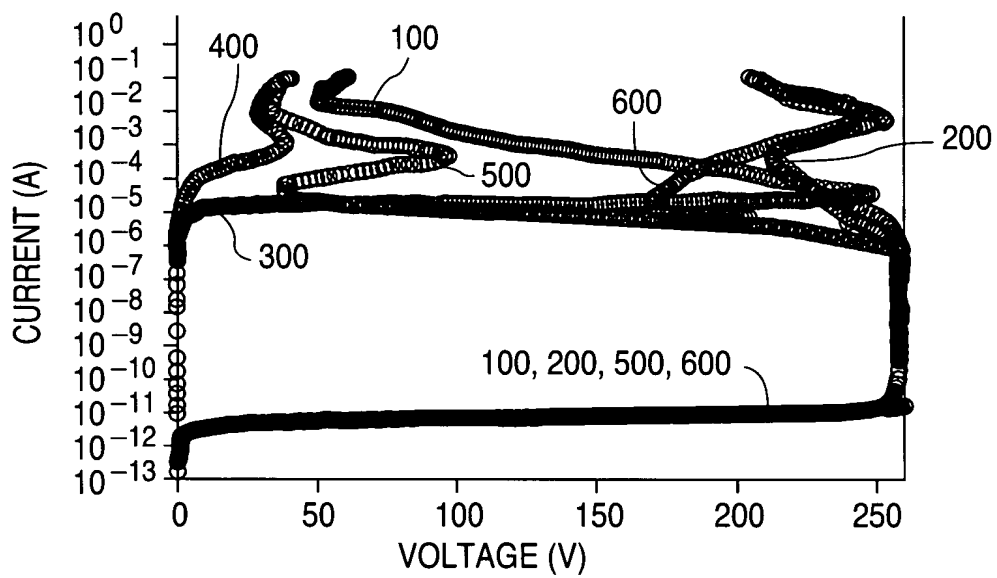


FIG. 5A

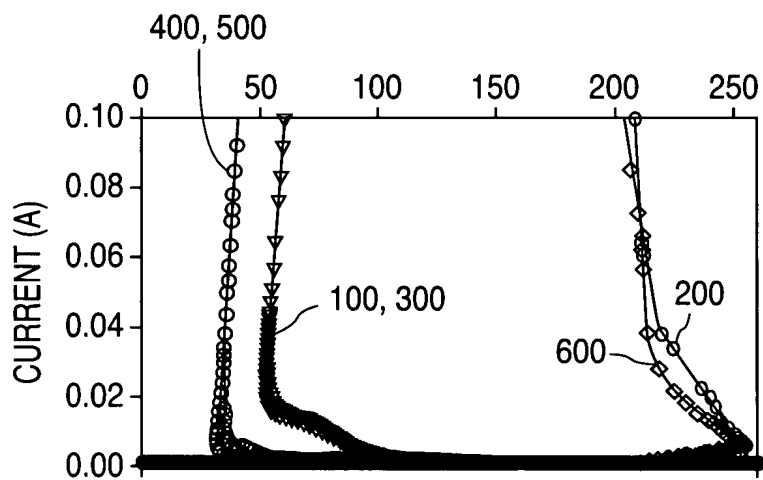


FIG. 5B

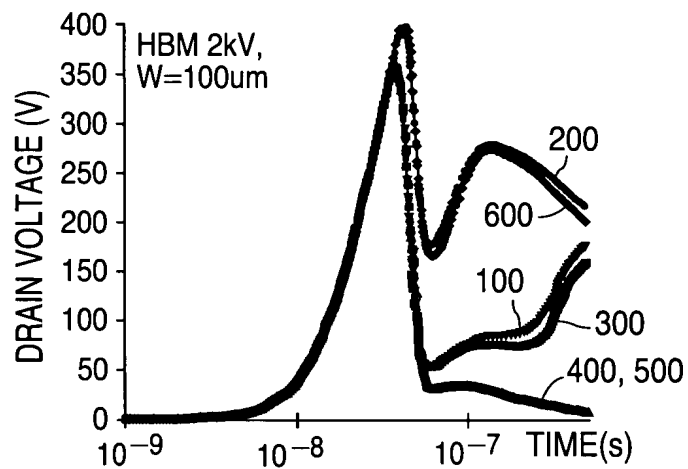


FIG. 5C

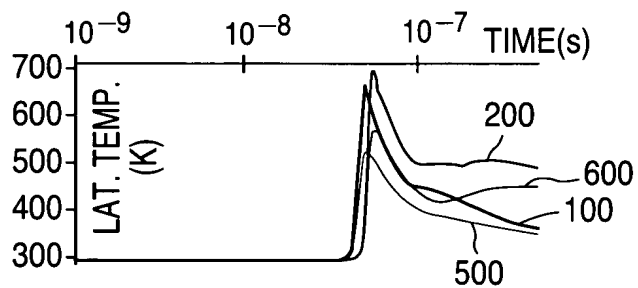


FIG. 5D

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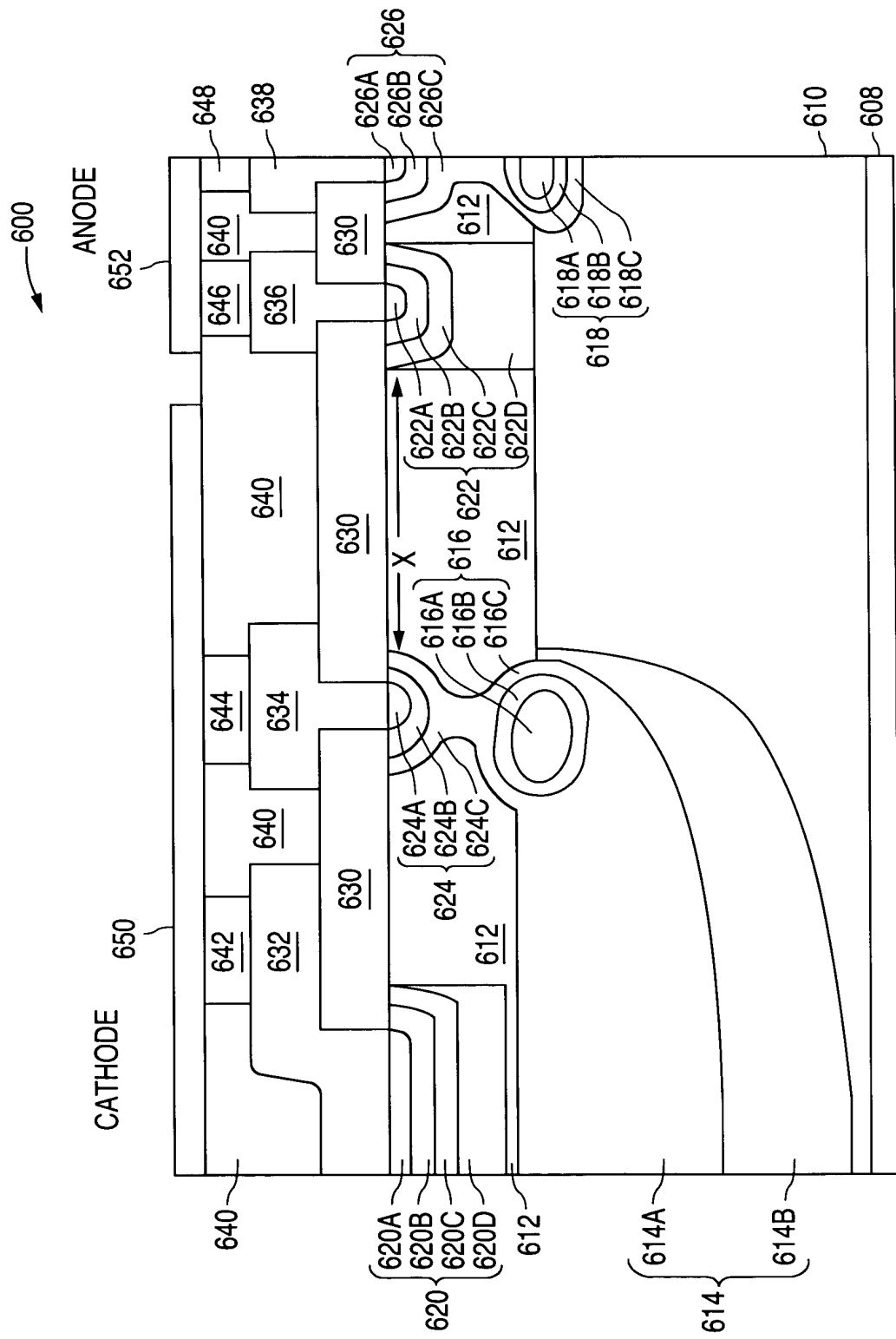
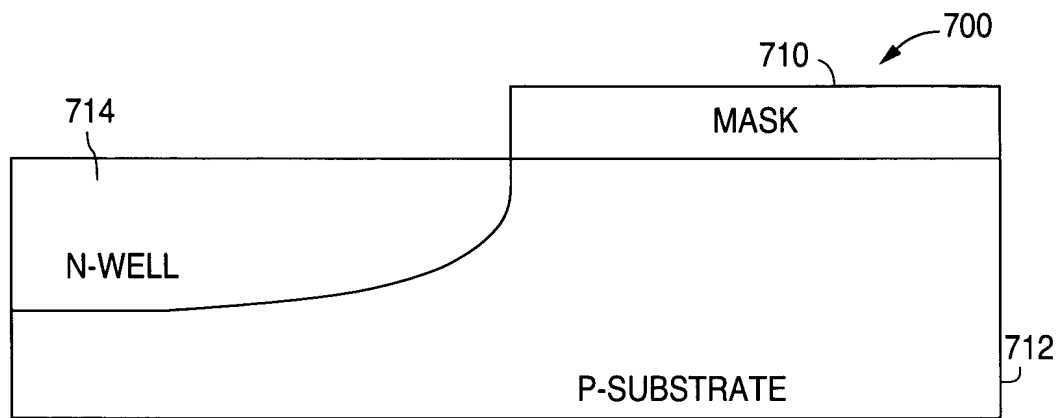
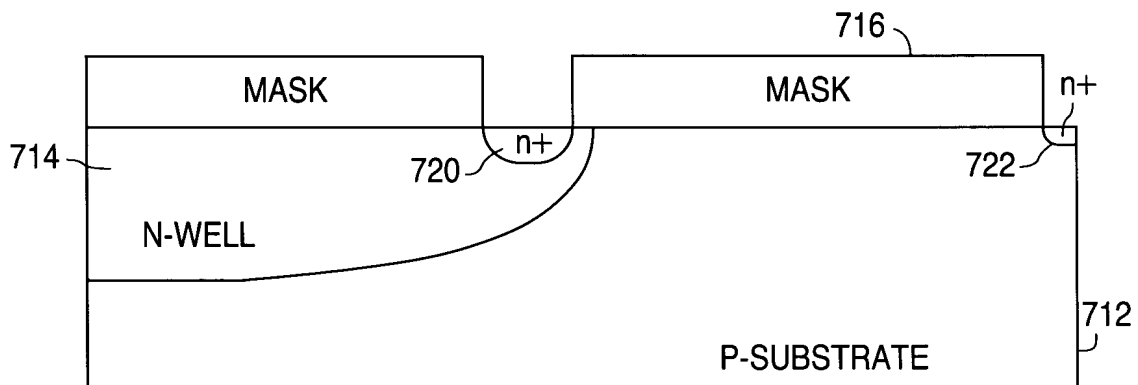


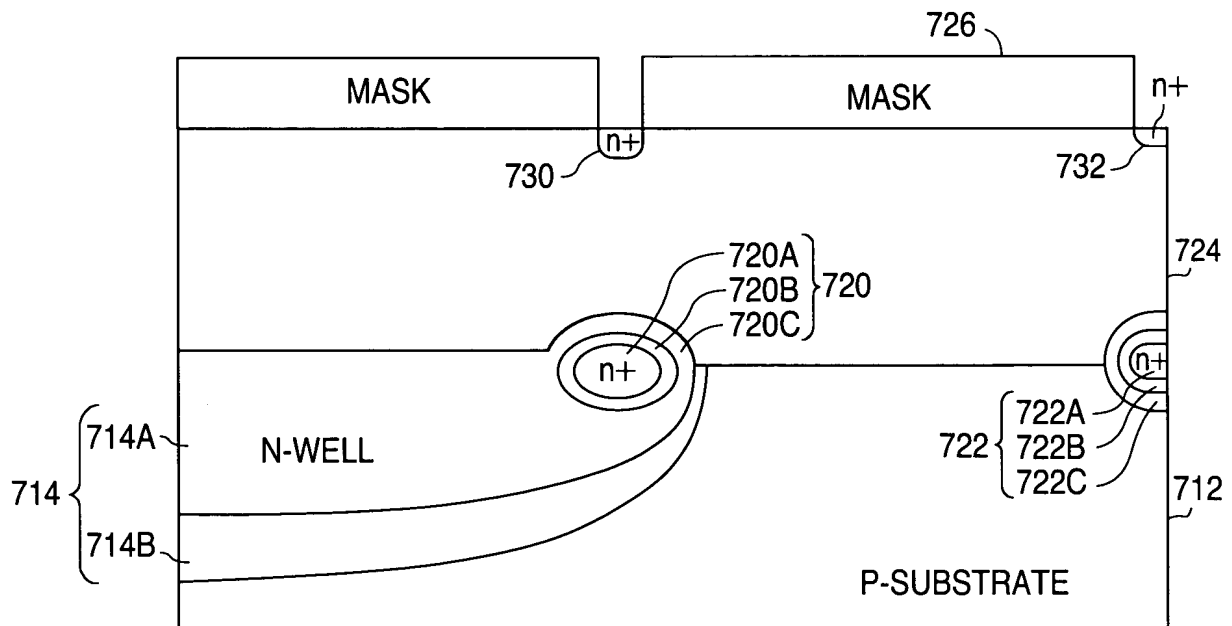
FIG. 6



**FIG. 7A**



**FIG. 7B**



**FIG. 7C**



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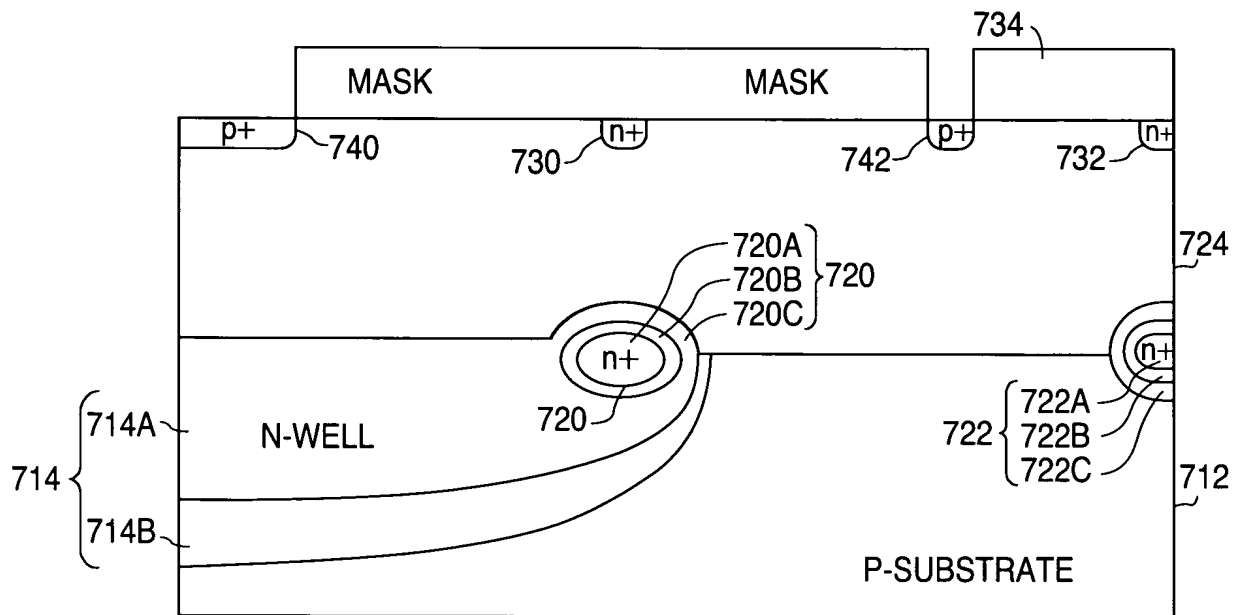


FIG. 7D

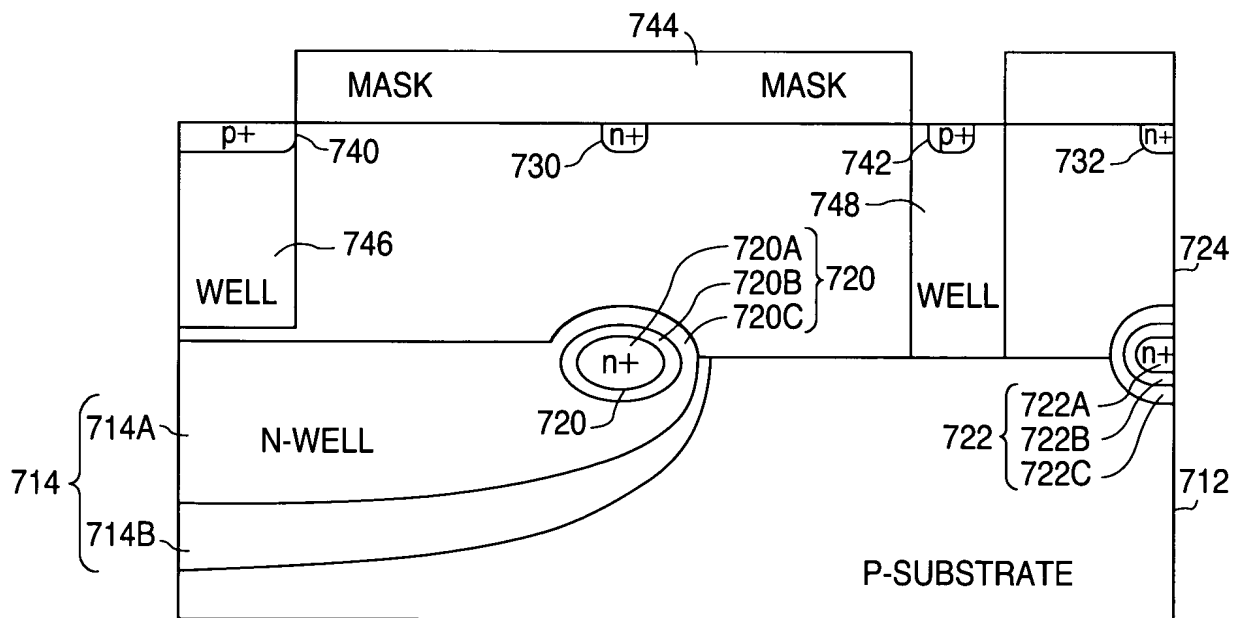


FIG. 7E

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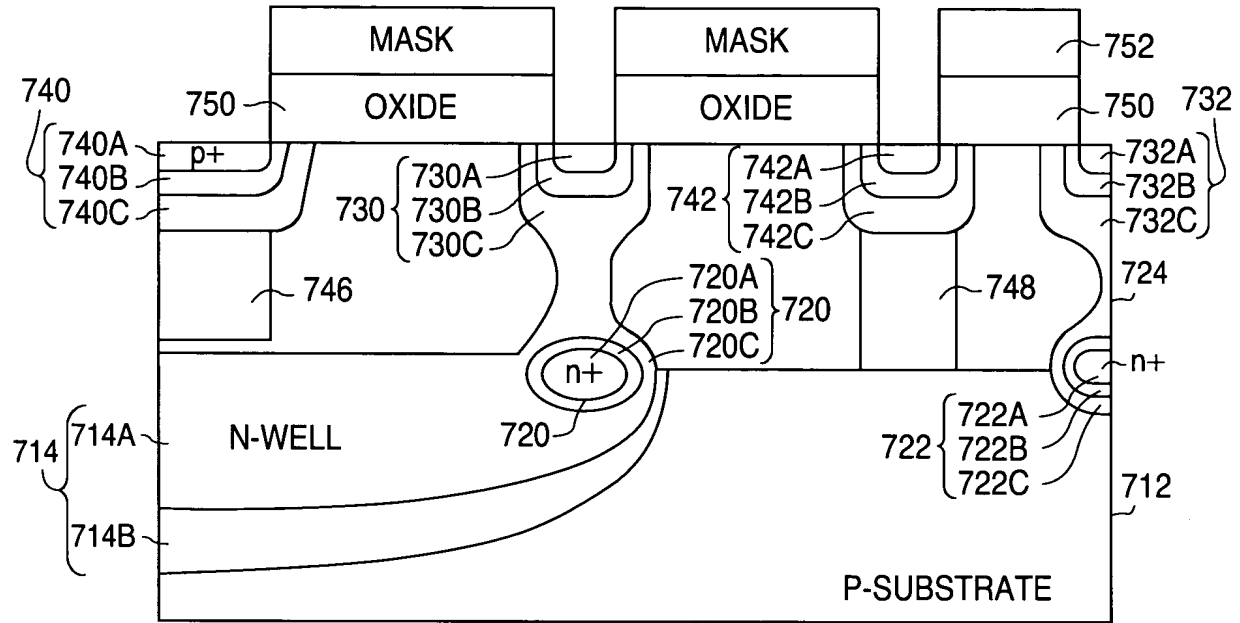


FIG. 7F

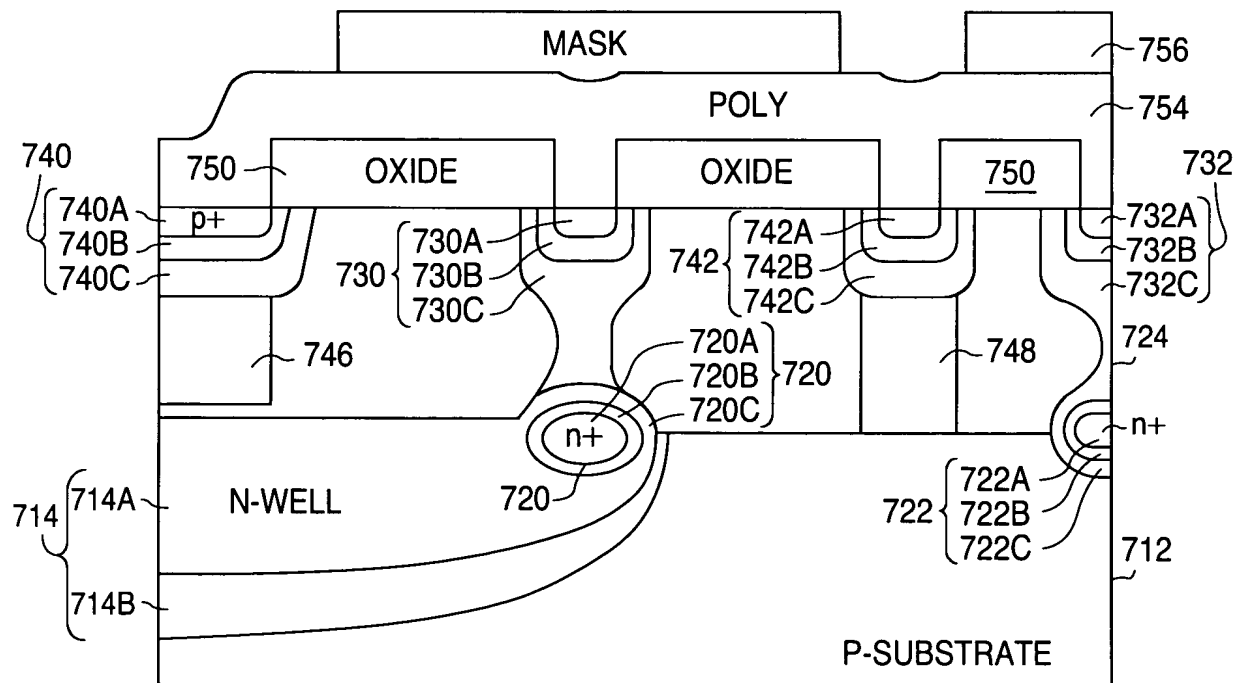
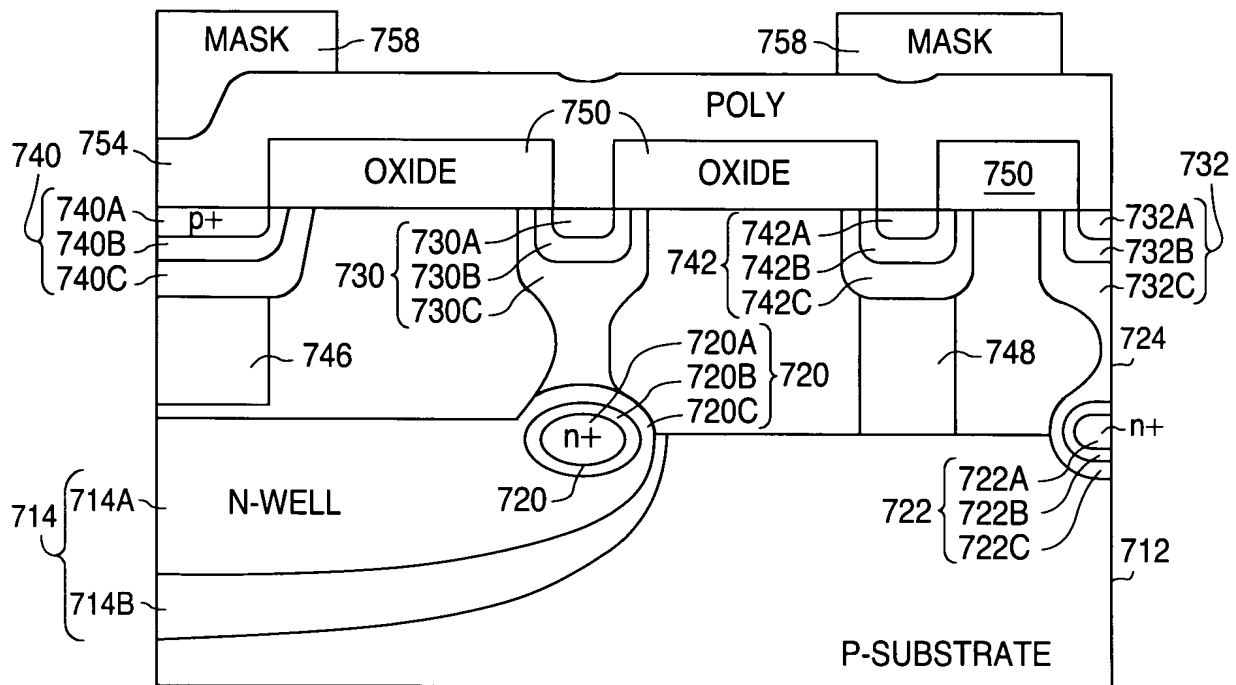
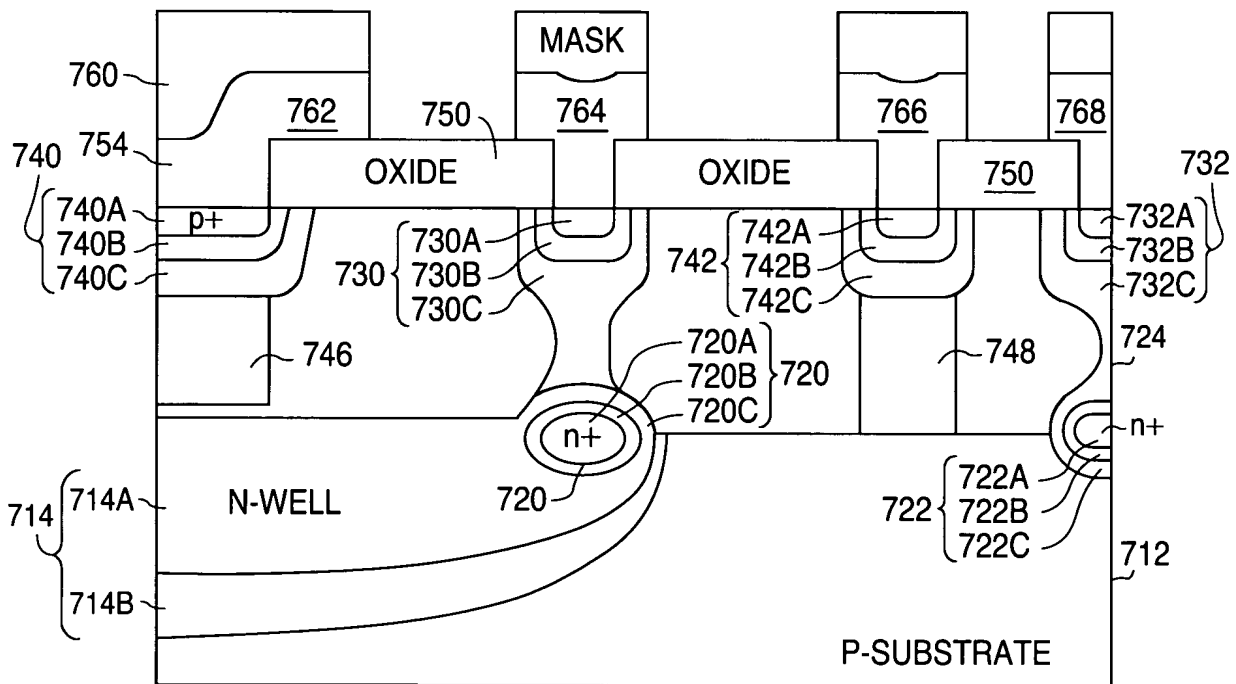


FIG. 7G



**FIG. 7H**



**FIG. 7I**

A detailed cross-sectional view of a semiconductor device. The structure is built on a P-SUBSTRATE. An N-WELL is formed in the substrate, containing an n+ region (720) with sub-layers 720A, 720B, and 720C. A p+ region (740) is also present, with sub-layers 740A, 740B, and 740C. Various oxide layers (750, 762, 764, 766, 768) and mask layers (770, 771) are shown. Other labeled regions include 730 (730A, 730B, 730C), 742 (742A, 742B, 742C), 722 (722A, 722B, 722C), 746, 748, 724, and 712. The device is bounded by a vertical line 714 on the left and 712 on the right.

782 MASK

780 METAL-1 784 786

770 772 770 774 770 776 770 778

754 762 750 764 750 766 768

740 754 OXIDE OXIDE 750 732

740A p+ 730A 742A 732A

740B 730B 742B 732B

740C 730C 742C 732C

746 720A 720B 720C 748 724

720 n+ n+

714 714A N-WELL 722A 722B 722C 712

714B P-SUBSTRATE